High Speed 10-Bits LVDS Receiver
EP104

User Guide
V0.7

Revised: Mar 12, 2007

Original Release Date: Aug. 10, 2004

Explore Microelectronics Inc.

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Aug/10/2004	Ether Lai	Initial Version
0.1	Oct/28/2004	Ether Lai	Add Power Consumption; Add Package;
0.2	Feb/17/2005	Ether Lai	Add maximum power dissipation & thermal resistance
0.3	Apr/13/2005	Ether Lai	Add Electrical Characteristics
0.4	Jun/01/2005	Ether Lai	Describe the reserved "FILTb" ("TEST")pin function
0.5	Aug/23/2006	Haowen Lu	Add set-up and hold time information of AC specification
0.6	Sep/25/2006	Haowen Lu	Add T_{cdelay} information
0.7	Mar/12/2007	Haowen Lu	Change support clock range

Section 1 Introduction

1.1 Overview

The EP104 supports single link transmission between the host and the flat panel display up to SXGA+ resolution. The EP104 converts the LVDS differential inputs into 35-bits control and data outputs. Also, the output data can be aligned to the rising or the falling edge of the output clock.

1.2 Features

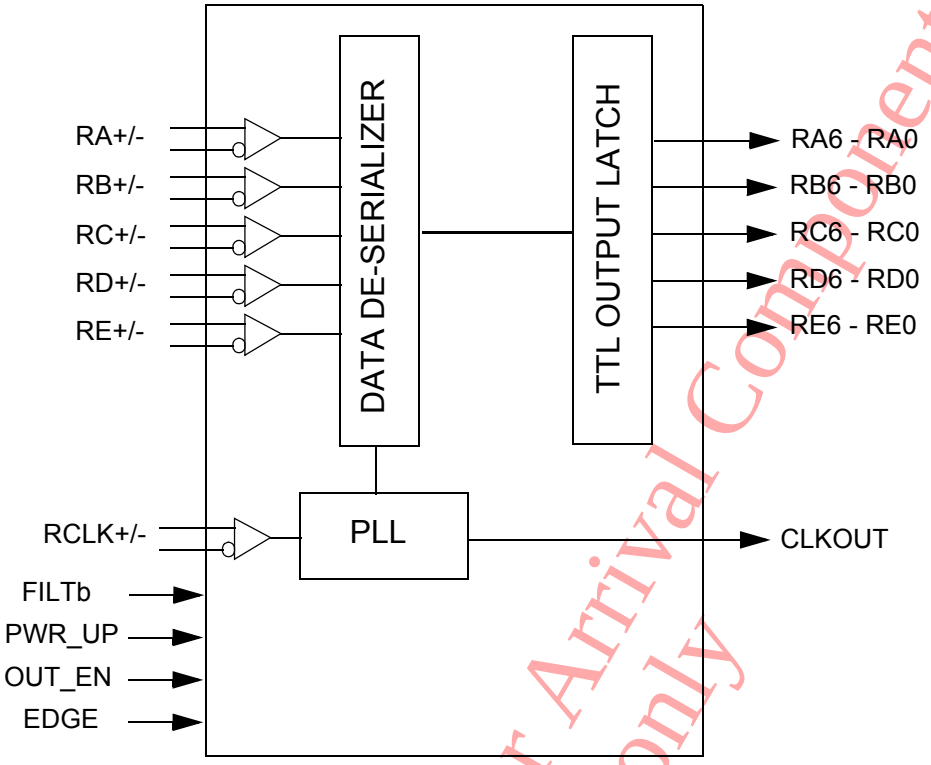
The EP104 includes the following distinctive features:

- Supports clock range from 8MHz to 90MHz
- PLL requires no external components
- Output Clock Edge Programmable
- Power Down Mode
- Compatible with THine THC63LVD104
- Single 3.3V CMOS design
- 64-pin LQFP (Pb-free)

Section 2 Overview

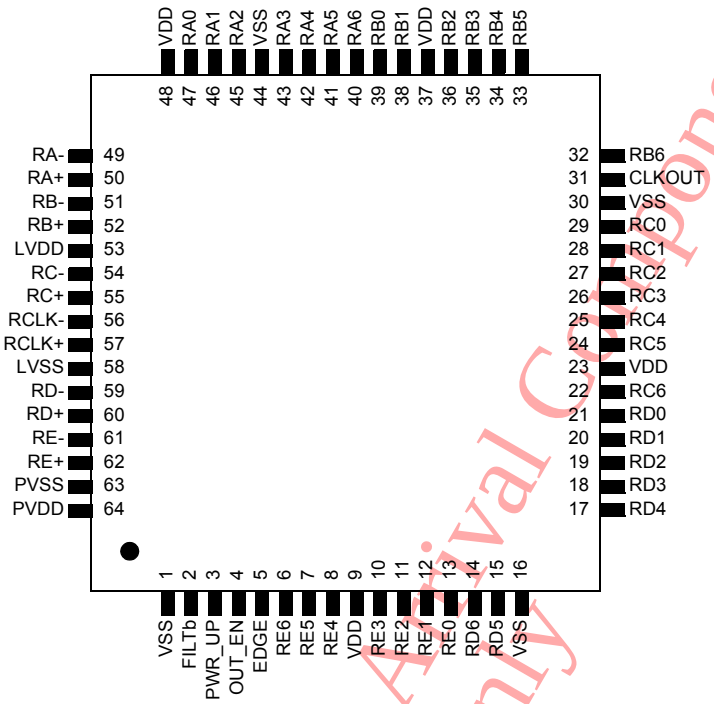
2.1 Block Diagram

Figure 2-1 Block Diagram of LVDS Receiver EP104



2.2 Pin Diagram

Figure 2-2 Pin Diagram of EP104



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Digital I/O Pins of EP104

NAME	PIN #	IN/OUT	DESCRIPTION
RA6~RA0	40-43, 45-47	OUT	Digital Data Outputs
RB6~RB0	32-26, 38,V39		
RC6~RC0	22, 24-29		
RD6~RD0	14, 15, 17-21		
RE6~RE0	6-8, 10-13		
CLKOUT	31	OUT	Data Clock Output.
PWR_UP	3	IN	H : Normal Operation L : Power Down Mode
OUT_EN	4	IN	H : Enable Output L : Disable Output (tri-stated)
EDGE	5	IN	H : Output Data Triggered by Rising Edge of CLKOUT L : Output Data Triggered by Falling Edge of CLKOUT
FILTb	2	IN	The H/V/DE signal with pulse width less than 8 clocks will be screened out if the Filter Function is enabled. H : Filter Function Disabled. L : Filter Function Enabled. Recommend to tie to "LOW" for Normal Operation

Table 2-2 LVDS Input Pins of EP104

NAME	PIN #	IN/OUT	DESCRIPTION
RA-, RA+	49, 50	IN	LVDS differential data input.
RB-, RB+	51, 52		
RC-, RC+	54, 55		
RD-, RD+	59, 60		
RE-, RE+	61, 62		
RCLK-, RCLK+	56, 57	IN	LVDS differential clock input.

Table 2-3 Power and Ground Pins of EP104

NAME	PIN #	IN/OUT	DESCRIPTION
VDD	9, 23, 37, 48	PWR	Digital VDD, 3.3V
VSS	1, 16, 30, 44	GND	Digital Ground.
LVDD	53	PWR	Analog VDD, 3.3V
LVSS	58	GND	Analog Ground.
PVDD	64	PWR	PLL VDD, 3.3V
PVSS	63	GND	PLL Ground.

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc[1]	Supply Voltage	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O[2]	Output Voltage	-0.3		V_{cc} + 0.3	V
V_{ID}	LVDS Driver Input Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature	-25		125	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		56.82		°C/W

NOTES:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	-10	25	70	°C

CMOS/TTL DC Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0		Vcc	V
V_{IL}	Low-level Input Voltage		GND		0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = -2 mA	2.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2 mA			0.4	V
I_{INC}	Input Current	0 <= V_{IN} <= Vcc			+/- 10	uA

LVDS Receiver DC Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{OC} = 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{OC} = 1.2V	-100			mV
I_{INL}	Input Current	V_{IN} = 2.4V/ 0V, V_{DD} = 3.6V			+/- 20	uA

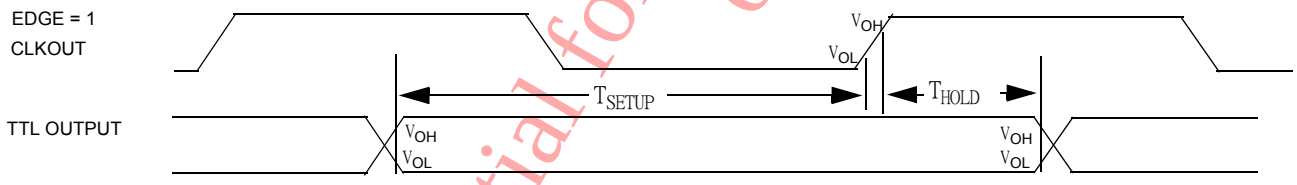
Supply Current (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{RCCG}	Receiver Supply Current	C_L = 10 pF, 256 Grayscale Pattern	F = 65 MHz		38	53	mA
			F = 90 MHz		45	67	mA
		C_L = 10 pF, Worst Case Pattern[1]	F = 65 MHz		66	95	mA
			F = 90 MHz		85	131	mA
I_{RCCZ}	Receiver Power Down Current	PWR_UP = 0			5	10	uA

NOTES:
1. Black and White checkboard pattern, each checker is 1 pixels wide.

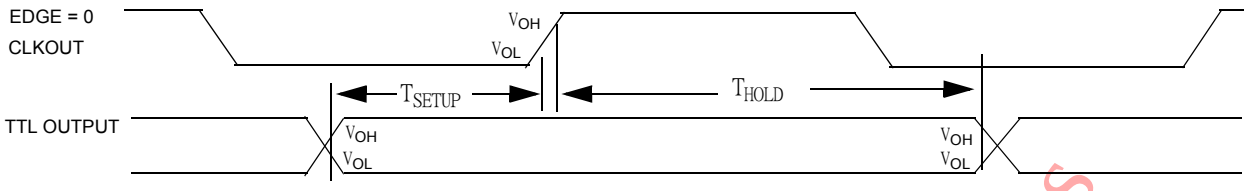
AC Specifications (under normal operating conditions unless otherwise specified**)**

Data Output at CLKOUT Rising Edge



Symbol	Parameter	Conditions		Min	Typ	Max	Units
T_{SETUP}	Setup time	V_{CC} = 3.3V	CLK=75MHz	8.4	12		nS
T_{HOLD}	Hold time	V_{CC} = 3.3V	CLK=75MHz	1.03	1.475		nS

Data Output at CLKOUT Falling Edge

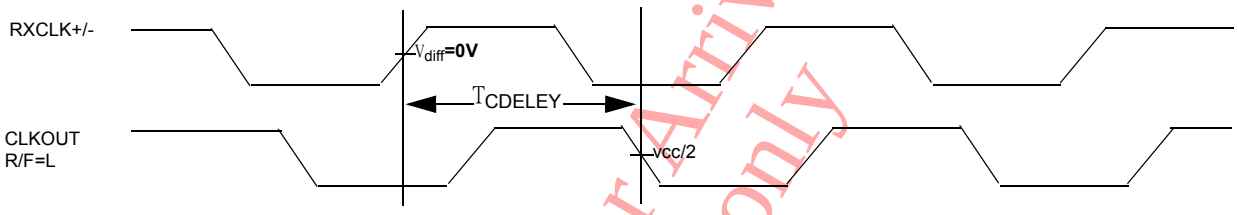


Symbol	Parameter	Conditions		Min	Typ	Max	Units
T_{SETUP}	Setup time	V_{CC} = 3.3V	CLK=75MHz	4.14	4.98		nS
T_{HOLD}	Hold time	V_{CC} = 3.3V	CLK=75MHz	7.49	8.32		nS

Notes:

1.T_{setup} is defined assuming next stage input samples the TTL outputs from EP104 at the rising edge of CLKOUT.

T_{CDELEY}



Symbol	Parameter	Conditions		Min	Typ	Max	Units
T_{CDELEY}	RXCLK+/- TO CLKOUT DELAY	V_{CC} = 3.3V	CLK=75MHz	42.2		46.2	nS

2.5 LVDS Outputs / TTL Data Inputs Mapping

The LVDS Clock waveshape is shown in the following figure. Note that the rising edge of the LVDS clock occurs two LVDS sub symbols before the current cycle of data. The clock is composed of a 4 LVDS sub symbol HIGH time and a 3 LVDS sub symbol LOW time.

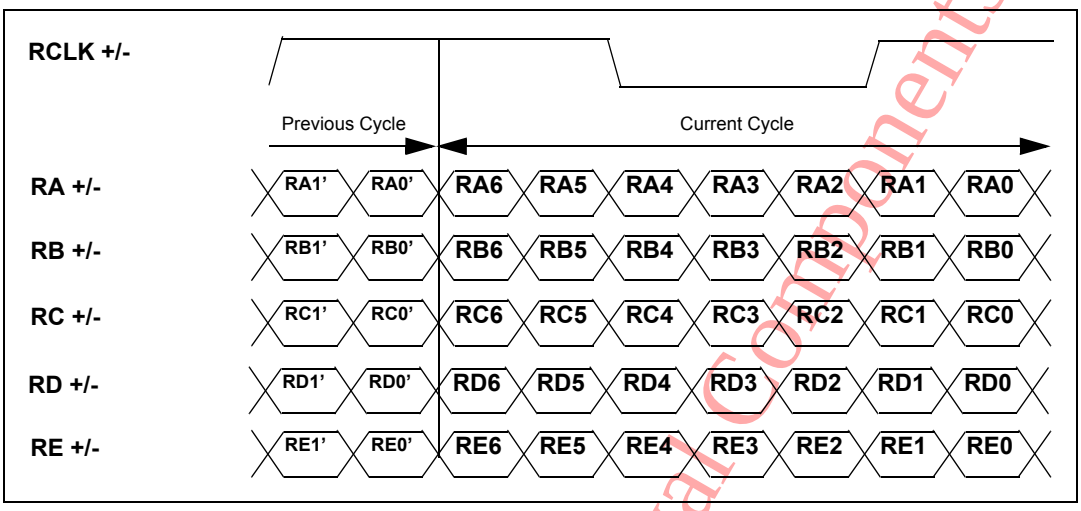
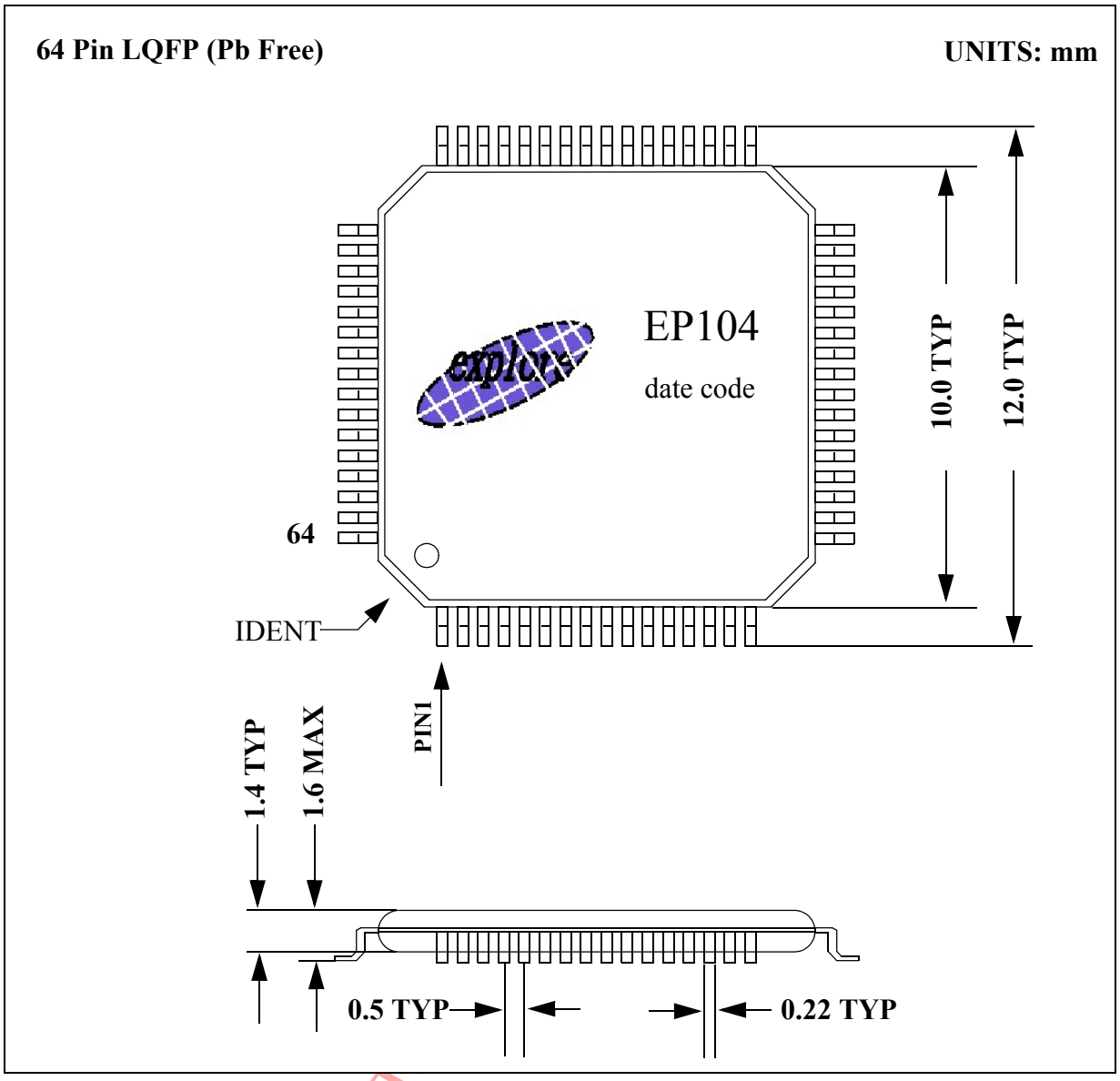


Figure 2-3 LVDS Inputs / TTL Outputs Data Mapping

2.6 Package



User Guide End Sheet

FINAL PAGE OF
14
PAGES