3 Ghz HDMI Repeater with 4K2K Scaler, Re-Timed Audio and Dual HDMI Outputs

EP91Z2E

Data Sheet V0.3

Revised Date: July. 26, 2013
Original Release Date: Dec. 06, 2012

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Jun/21/2013	Ken Chen	Initial Version
0.2	Jun/21/2013	Ken Chen	Revise the 1.8V Range;
0.3	July/26/2013	Ken Chen	Integrate the Design Guide;

Section 1 Introduction

1.1 Overview

EP91Z2E is a 3 Ghz HDMI Repeater with 4K2K Scaler, Re-Timed Audio and dual HDMI outputs. The chip supports one 3 Ghz HDMI port and two 3 Ghz HDMI TX ports with Video Scaling, Audio Re-Timing and HDCP Repeater function.

The on-chip Video Up/Down Scaler can convert video input stream from 1080p to 4K2K or from 4K2K to 1080p. The Re-Timed Audio can convert video timing mode (register programmable) and keep audio stream intact.

Each HDMI TX port can be configured to output Scaled Video, Re-Timed Audio or by-pass AV stream from HDMI RX port.

The chip is compliant with HDMI 1.4 and supports SD/HD Audio and HD/3D/4K2K Video. The chip also supports on-chip HDCP RX/TX engines and EDID RAM.

The chip also integrated with a eFlash MCU to make user's applications very easy.

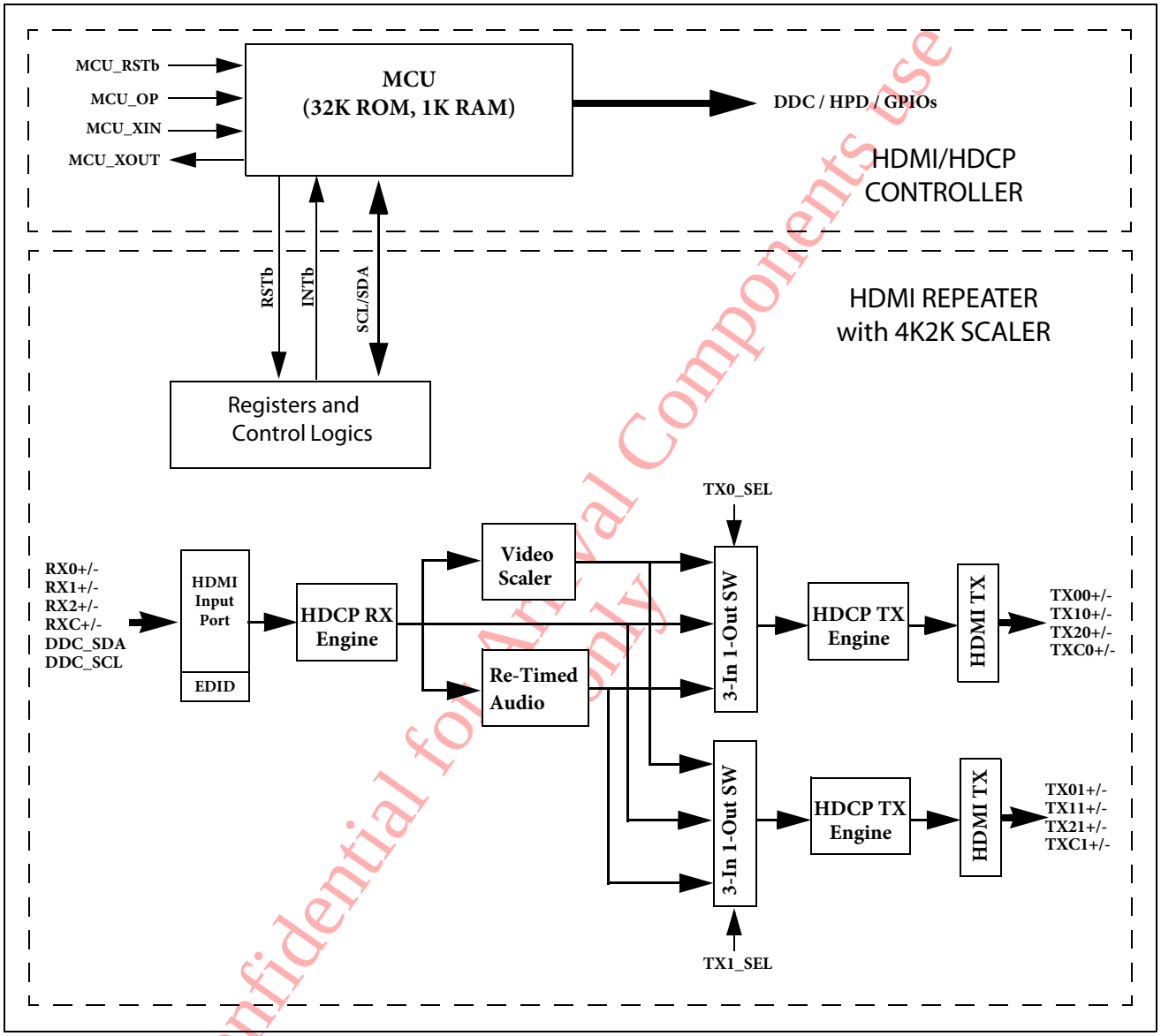
1.2 Features

- On-chip HDMI Receiver core which is compliant with HDMI 1.4 specification
- On-chip HDMI Transmitter core which is compliant with HDMI 1.4 specification
- Support 1 HDMI RX port and 2 HDMI TX ports
- Both HDMI RX and TX support TMDS clock rate up to 300 Mhz
- On-chip HDCP RX/TX Engine which is compliant with HDCP 1.4 specification
- On-chip Video Up/Down Scaler which can convert video input stream from 1080p to 4K2K or from 4K2K to 1080p
- Programmable Image Processing capability for 4K2K Scaler
- On-chip Re-Timed Audio which can convert video timing mode (register programmable) and keep audio stream intact.
- Flexible output configuration. Each HDMI TX port can be configured to output Scaled Video, Re-Timed Audio or bypass AV stream from HDMI RX port.
- On-chip EDID RAM
- On-chip eFlash MCU with integrated HDCP keys
- Support HDMI Repeater function
- Low stand-by current (< 1mA) at power down mode
- 80-pin LQFP package

Section 2 Overview

2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 EP91Z2E Pin Diagram (LQFP-80)

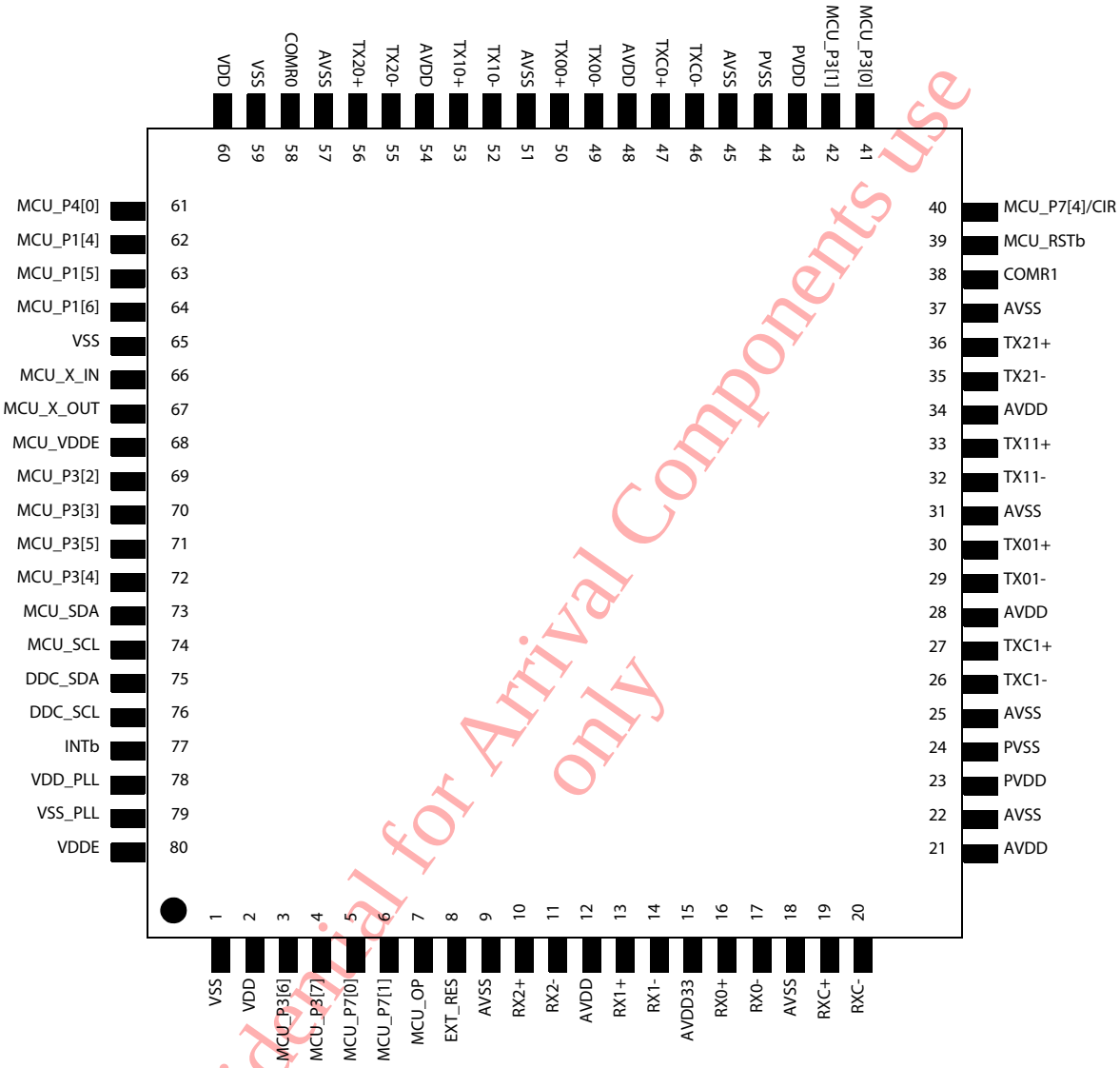


Figure 2-2 EP91Z2E Pin Diagram

2.3 Pin Description

Table 2-1 HDMI Input Port

Name	In/Out	Description
RXC-	IN	HDMI Receiver Differential Clock Input Pair
RXC+	IN	HDMI Receiver Differential Clock Input Pair
RX0-	IN	HDMI/MHL Receiver Differential Data Input Pair1
RX0+	IN	HDMI/MHL Receiver Differential Data Input Pair1
RX1-	IN	HDMI Receiver Differential Data Input Pair1
RX1+	IN	HDMI Receiver Differential Data Input Pair1
RX2-	IN	HDMI Receiver Differential Data Input Pair2
RX2+	IN	HDMI Receiver Differential Data Input Pair2
EXT_RES	IN	External Termination Resistor. A resistor should tie this pin to AVDD33. 470Ω is recommended.
DDC_SCL	IN	IIC SCL signal for HDMI RX DDC Port
DDC_SDA	IO	IIC SDA signal for HDMI RX DDC Port

Table 2-2 HDMI Output Port 0

Name	In/Out	Description
TXC0-	OUT	Differential Clock Output Pair for HDMI Output 0
TXC0+	OUT	Differential Clock Output Pair for HDMI Output 0
TX00-	OUT	Differential Data Output Pair0 for HDMI Output 0
TX00+	OUT	Differential Data Output Pair0 for HDMI Output 0
TX10-	OUT	Differential Data Output Pair1 for HDMI Output 0
TX10+	OUT	Differential Data Output Pair1 for HDMI Output 0
TX20-	OUT	Differential Data Output Pair2 for HDMI Output 0
TX20+	OUT	Differential Data Output Pair2 for HDMI Output 0
COMR0	Analog	Common ground for pull-down resistors for HDMI Output 0

Table 2-3 HDMI Output Port 1

Name	In/Out	Description
TXC1-	OUT	Differential Clock Output Pair for HDMI Output 1
TXC1+	OUT	Differential Clock Output Pair for HDMI Output 1
TX01-	OUT	Differential Data Output Pair0 for HDMI Output 1
TX01+	OUT	Differential Data Output Pair0 for HDMI Output 1
TX11-	OUT	Differential Data Output Pair1 for HDMI Output 1
TX11+	OUT	Differential Data Output Pair1 for HDMI Output 1
TX21-	OUT	Differential Data Output Pair2 for HDMI Output 1
TX21+	OUT	Differential Data Output Pair2 for HDMI Output 1
COMR1	Analog	Common ground for pull-down resistors for HDMI Output 1

Table 2-4 Misc. Pins

Name	In/Out	Description
MCU_SCL	IN	SCL signal for slave IIC port
MCU_SDA	IO	SDA signal for slave IIC port

Table 2-5 HDMI Controller Pins

Name	In/Out	Description
MCU_RSTb	IN	External Reset (active low) with on-chip pull-up. When this pin is asserted low, the HDMI controller is totally reset.
MCU_OP	IN	HDMI Controller operation mode 0: Normal mode 1: ICP (In Circuit Flash Programming) mode
MCU_X_IN	IN	External Crystal Input, 24 MHz
MCU_X_OUT	OUT	External Crystal Output, 24 MHz
P1[6:4]	IN/OUT	GPIO port 1 or Keyboard Interrupt inputs with internal 20KΩ pull-up to MCU_VDDE
P4[0]	IN/OUT	GPIO port 4 or External Interrupt inputs
P3[7:0]	IN/OUT	Open Drain I/O port 3, shared with IIC Port
P7[1:0]	IN/OUT	Open Drain I/O port 7, shared with Serial Port
P7[4]/CIR	IN/OUT	Open Drain I/O port 7, shared with CIR Port

Table 2-6 Power Pins

Name	In/Out	Description
AVDD33	PWR	HDMI Termination Power (3.3V)
AVDD	PWR	HDMI RX/TX Analog Power (1.8V)
AVSS	GND	HDMI RX/TX Analog Ground
PVDD	PWR	HDMI RX/TX PLL Analog Power (1.8V)
PVSS	GND	HDMI RX/TX PLL Analog Ground
VDDE	PWR	Digital I/O Power (3.3V)
VDD	PWR	Core Logic Power (1.8V)
VSS	GND	Core Logic Ground
VDD_PLL	PWR	PLL VDD (1.8V)
VSS_PLL	GND	PLL Ground
MCU_VDDE	PWR	HDMI Controller Power (3.3V)

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc33} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc33} + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		44		°C/W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	2.1[1]	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

NOTES:
1. Analyzed by FEB (Finite Element Modeling) method with chip mouted on 4-layers PCB.

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Output Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V; TX_TERM bit is 0				5	uA
I_{PD}	Power-Down Current[2]	25°C Ambient	3V3		21		uA
			1V8		10.4		uA
I_{CCD}	Supply Current (25°C Ambient, R_{EXT_RES} = 470 ohm, R_{EXT_RES})	IN: 4K2K 24Hz OUT A: 4K2K 24Hz OUT B: 4K2K 24Hz	3V3[3]		65		mA
			1V8[4]		744		mA
		IN: 1080p 24Hz OUT A: 4K2K 24Hz OUT B: 4K2K 24Hz	3V3[3]		65		mA
			1V8[4]		700		mA

1 Guaranteed by design.
2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.
3 Including all the 3V3 power domain (AVDD33, VDDE).
4 Including the 1V8 power domain (AVDD, PVDD, VDD, VDD_PLL).

HDMI Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
F_{CIP}	TMDS CLK Frequency		25		300	MHz

NOTES:
1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronic Measurement Procedures*

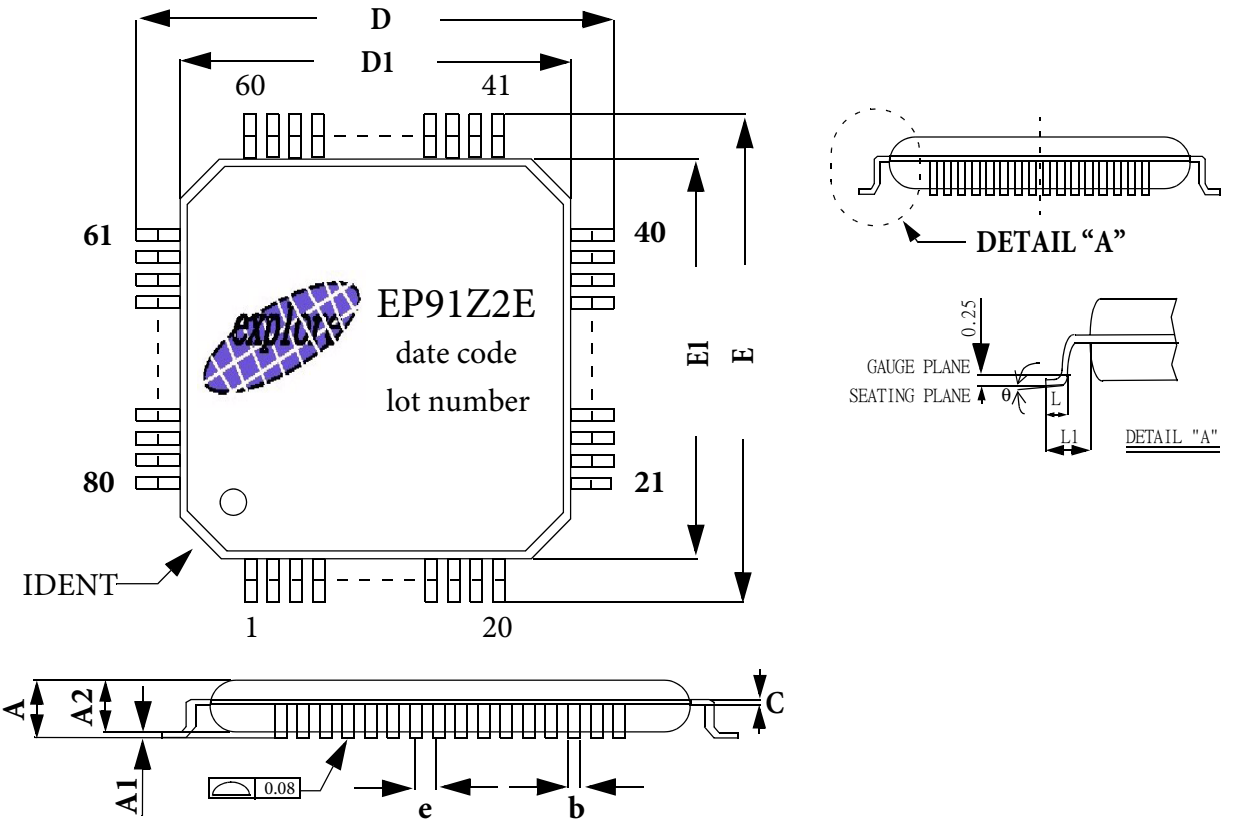
Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm	170	200	230	ps

S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm	170	200	230	ps

Appendix A Package

Figure A-1 EP91Z2E Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
C	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

Appendix B EP91Z2 Application Guideline

This application note describes the guideline for the system designer to follow while preparing the application circuit and PCB layout in order to achieve the best performance of the EP91Z2.

B.1 GENERIC DESIGN GUIDELINE

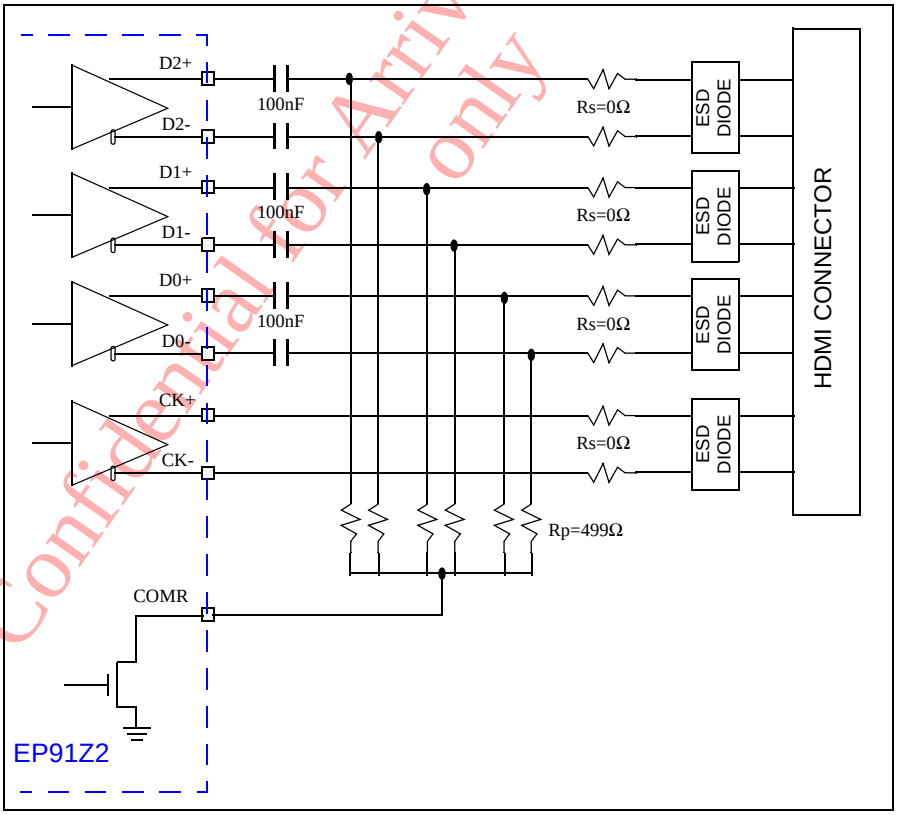
B.1.1 HDMI Receiver

- For receiver input, each differential pair shall be routed symmetrically. Also, the best performance will be expected if the differential pair is equal length. The maximum difference of the trace length between D+ and D- (intra-pair) is 12 mil.
- The receiver module can tolerate the skew among different pairs (inter-pair skew). Anyway, user can limit the maximum difference of the trace length among different pairs (inter-pair) to 150 mil.

B.1.2 HDMI Transmitter

The transmitter uses the new AC-coupling mechanism at its differential data output. The block diagram of the recommended transmitter output connection is shown in the following figure.

Figure B-1 Transmitter Output Connection

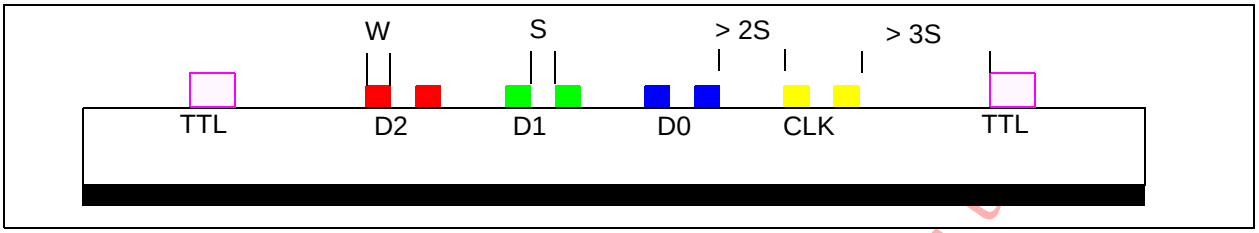


- The 100nF capacitor to implement the AC-coupling mechanism is needed for the TMDS differential data output. The differential clock output still keeps the DC-coupling mechanism.
- The 499Ω (Rp) pull down resistor for each differential data output signal is needed for keeping the DC voltage to the TMDS connector output to be 3V3.
- In order to provide the higher level of the ESD protection in the HDMI TX output, a serial resistor (Rs) can be added between the external ESD device and the silicon HDMI transmitter output pad. The typical value of the serial resistor could be set to 0Ω first.
- For transmitter output, each differential data pair shall be routed symmetrically. The best performance will be expected if the differential data pairs are equal length. The maximum trace difference will depends on the connected receiver characteristics. In practice, try to minimize of the trace length differences of the intra-pair and inter-pairs of the differential data lines.
- For the best intra-pair skew between the single-ended CLK+ output and single-ended CLK- output, it is recommended to route the CLK+ with the trace length longer than CLK- for 400 mil to 600 mil. Keep the area of the CLK+ and CLK- current loop to have the minimum area while routing the additional trace of the CLK+ signal.
- Minimize the length from the HDMI TX pins to the HDMI connector. If possible, keep the length less than 1500 mil.

B.2 GENERIC LAYOUT GUIDELINE

- PVDD for TMDS transmitter shall be applied with the clean power, the common practice is to supply the power through the ferrite bead. The best practice is to provide the PVDD through the individual regulator. The minimum requirement is to follow the reference circuit to supply the power to PVDD.
- In order to provide a desirable return path for current, the solid ground plane is necessary. Also, connect the power and ground pins and all bypass capacitors to the appropriate power and ground plane with a via. Via is suggested to be as fat and as short as possible in order to reduce the inductance.
- Place one 0.1uF capacitor as close as possible between each power pin and ground. A bulk decoupling capacitor should be placed on the sub-plane of the power. Additional capacitors may be needed depending on the PCB design.
- Control the PCB impedance of all differential traces (both receiver and transmitter) to be 100Ω. This will be one of the critical points for the system performance at very high frequency operation. Following items are listed based on our experience:
  - If possible, the differential traces shall be routed on the TOP layer and the continuous ground plane shall be placed beneath the differential traces. The discontinuous ground plane will degrade the high speed differential signal integrity.
  - The ground traces stay with the differential traces on the same layer are not suggested.
  - Keep any TTL signals away from the differential traces as far as possible.
  - Avoid the differential traces cornering, crossing and the through holes.

- Choose the discrete ESD protection devices with the very low capacitance, the Semtech RClamp0524P or CMD (California Micro Devices) CM2020 is recommended. Place the ESD devices close to the HDMI connector for the best performance.
- Following diagram shows the differential traces routing example:



B.3 Heat Transfer

While all HDMI Transmitter Ports are turned on, the power consumption of the chip will increased significantly. From the measurement in typical conditions (Room Temperature, 1V8 and 3V3 supply voltage), this silicon will consume up to 1.5 Watt if all the two transmitter ports are all powered on at the 4Kx2K resolution which the pixel clock frequency is up to 297MHz.

Considering this high current consumption application, engineer shall be very careful while designing the heat transfer mechanism. Additional mechanisms to remove the heat from the internal silicon from the package shall be considered too. For example, additional heat sink or thermal cooling fan may be considered.

Besides, the choice to the supplied power generation will be very important. There are two kinds of regulators are widely used in current market, the switching type regulator provides high efficiency and high power density but it also induces more ripples to the output. The LDO regulator has the less efficiency but it provides the smaller ripple to the output. While choosing the LDO as the target regulator, lots of energy will be consumed during the regulation, especially for the conversion from 5V to 1V8. The similar criterion to take care of the heat removal from the LDO shall be considered too.